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Description

[SPLIT GATE FLASH MEMORY CELL AND MANUFACTURING METHOD THEREOF]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92122059, filed on August 12, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to a fabrication method for a capacitor. More particularly, the present invention relates to a buried plate of a deep trench capacitor.

[0004] Description of Related Art

[0005] As semiconductor devices enter the deep sub-micron processing, the device dimension gradually reduces. For a dynamic random access memory (DRAM) device, the area for forming the capacitor also diminishes. On the other hand, as the application of software increases, the memory capacity required by a memory device gradually in-

creases. When the demands on a smaller device dimension and a larger memory capacity become higher, it is obvious that the fabrication method for a capacitor of a DRAM device needs to the modified.

[0006] The structure of a DRAM capacitor is mainly divided into two types. One type is the stack capacitor, while the other is the deep trench capacitor. For a deep trench capacitor, increasing the capacitance of the capacitor within a limited area can be achieved by increasing the contact area of the electrode. Therefore, a bottle-shaped deep trench structure is typically used in a deep trench capacitor. Since the bottle-shaped deep trench can increase the area of the buried plate, the capacity of the capacitor also increases.

[0007] Figures 1A to 1E are schematic, cross-sectional view diagrams illustrating the process flow for fabricating a buried plate of a deep trench capacitor.

[0008] Referring to Figure 1A, a substrate 100 is provided, wherein a patterned mask layer 101 is formed on the substrate 100. The mask layer 101 comprises an opening which exposes a surface of the substrate 100. Using the mask layer 101 as an etching mask, an etching is conducted to pattern the substrate 100 to form a deep trench

102. An oxide layer 104 is further formed on the surface of the deep trench 102, except the top part of the trench 102. A nitridation process is subsequently conducted to form a silicon nitride layer 106 on the surface of the exposed substrate 100 in the deep trench 102.

[0009] Referring to Figure 1B, the oxide layer 104 is removed. Thereafter, wet etching is conducted to form a bottle-shaped deep trench 102a, wherein the part of the sidewall of the deep trench that is covered with a silicon nitride layer 106 is precluded from being wet etched.

[0010] Continuing to Figure 1C, the silicon nitride layer 106 is then removed. A conformal doped layer 108 is formed on the surface of the substrate 100 and on the surface of the deep trench 102a. A deep trench 102a is then filled with a photoresist layer 110, covering the doped polysilicon layer 108, wherein the photoresist layer 110 does not completely fill the deep trench 102a.

[0011] Referring to Figure 1D, the conformal doped layer 108, not covered by the photoresist layer is removed, leaving the doped layer 10a8 at the bottom of the deep trench 102a. The photoresist layer 110 is subsequently removed. A thermal process is further conducted to drive in the dopants in the doped layer 108a into the substrate 100 to

form a doped region 112, wherein the doped region 112 serves as the buried plate of the deep trench capacitor. Thereafter, the doped layer 108a in the deep trench 102a is removed as shown in Figure 1E to complete the fabrication of a buried plate of a deep trench capacitor.

[0012] In accordance to the above fabrication method, to complete the fabrication of a deep trench with a bottle shape structure requires multiple processing steps. Further, the bottle shape structure and the doped region (buried plate) are formed in different process steps. Therefore, the conventional fabrication process is very time-consuming. Moreover, the uniformity of the thickness of the photoresist layer, which is used to control the dimension of the buried plate, is difficult to control during the fabrication process. Consequently, the capacitance of the capacitor in the memory devices is not consistent. Further, forming the silicon nitride layer on the sidewall surface of the substrate is accomplished through a nitridation reaction. However, the desired thickness of the silicon nitride layer is difficult to control through a nitridation reaction. As a result, the silicon nitride layer formed according to the prior art is not effective in preventing the erosion of the etchant.

SUMMARY OF INVENTION

[0013] Accordingly, the present invention provides a fabrication method for a buried plate of a deep trench capacitor, wherein a non-uniform thickness of the photoresist, which is used to control the area of the buried plate, as in the prior art is obviated. Consequently, the area of the buried plate of the capacitor being inconsistent is prevented.

[0014] The present invention also provides a fabrication method for a buried plate of a deep trench capacitor for resolving the problem of an inadequate thickness of the silicon nitride layer formed on the sidewall surface of the substrate by the conventional nitridation reaction, wherein the inadequate thickness of the silicon nitride layer fails to obstruct the erosion of the etchant.

[0015] The present invention further provides a fabrication method for a buried plate of a deep trench capacitor for reducing the processing steps.

[0016] The present invention provides a fabrication method for a buried plate of a deep trench capacitor, wherein a deep trench is first formed in the substrate. A conformal dope layer is formed on the substrate and the surface of the deep trench. The deep trench is then filled with a material

layer, for example, a polysilicon material, wherein the material layer does not fill the trench completely. The conformal doped layer that is not covered by the material layer is removed. A deposition process is conducted on the substrate and the surface of the trench to form a conformal passivation layer, wherein the passivation layer is, for example, silicon nitride. The conformal passivation layer is etched back to form a passivation layer on the sidewall of the deep trench that is not covered by the material layer. The material layer is subsequently removed. Thereafter a thermal process is conducted to drive-in the dopants in the doped layer into the substrate to form a doped region. Concurrently, the doped layer would react with the substrate to form an oxide layer, wherein the doped region can serve as the buried plate of the deep trench capacitor.

[0017] Since the conventional photoresist layer is replaced by a polysilicon layer to control the dimension of the buried plate, the problem of having a non-uniform thickness in the photoresist layer as in the prior art is prevented. As a result, an inconsistency in the dimension of the buried plate can also be avoided.

[0018] Further, the passivation layer is formed on the sidewall of

the deep trench via a deposition process. The problem of having an inadequate thickness in the silicon nitride layer formed according to the conventional nitridation process, leading to a deficiency in preventing the erosion of the etchant is resolved.

[0019] Further, in accordance to the fabrication method of the present invention, the buried plate of the deep trench capacitor and the bottle-shaped deep trench structure for increasing the capacitance are concurrently formed to reduce the manufacturing time and to simplify the fabrication process.

[0020] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0021] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0022] Figures1A to 1E are schematic, cross-sectional view dia-

grams illustrating the process flow for fabricating a buried plate of a deep trench capacitor according to the prior art.

[0023] Figures 2A to 2H are schematic, cross-sectional view diagrams illustrating the process flow for fabricating a buried plate of a deep trench capacitor according to an aspect of the present invention.

DETAILED DESCRIPTION

[0024] Figures 2A to 2H are schematic, cross-sectional view diagrams illustrating the process flow for fabricating a buried plate of a deep trench capacitor according to one aspect of the present invention.

[0025] Referring to Figure 2A, a substrate 200 is provided. A patterned mask layer 202 is formed on the substrate 200, wherein the mask layer 202 is, for example silicon nitride. The mask layer 202 comprises an opening, which exposes the surface of the substrate. In one aspect of the invention, a pad oxide layer (not shown) can also be formed between the mask layer 202 and the substrate 200 to protect the surface of the substrate 200. Thereafter, the mask layer 202 is used as an etching mask to perform an etching process in which the substrate 200 is patterned to form a deep trench 204. The etching process includes, for example, a dry etching process. A conformal doped layer

206 is formed on the surface of the deep trench 204 and the mask layer 202, wherein the doped layer 206 is, for example, a silicate glass layer doped with arsenic ions, formed by, for example, a chemical vapor deposition method.

[0026] Referring to both Figure 2B and 2C, the deep trench 204 is filled with a material layer 208, covering a portion of the doped layer 206, wherein the material layer 208 does not completely fill the deep trench 204. The doped layer 206 not covered by the material layer 208 is removed to form the doped layer 206a. Forming the material layer 208 includes performing chemical vapor deposition to form a material layer (not shown) on the mask layer 202 and inside the deep trench, followed by removing a portion of the material layer to leave only the material layer inside the deep trench 204. The material layer is, for example, polysilicon. Thereafter, the conformal doped layer not covered by the material layer 208 is removed, for example, by a wet etching process, to form the doped layer 206a.

[0027] Referring to Figure 2D, a conformal passivation layer 210 is formed on the surfaces of the mask layer202 and the material layer 208, wherein the passivation layer 210 is,

for example, silicon nitride. Forming the conformal passivation layer includes, performing chemical vapor deposition. Further, the conformal passivation layer 210 is formed with a thickness of about 150 angstroms to about 200 angstroms.

[0028] Referring to both Figures 2E and 2F, the conformal passivation layer 210 is etched back to expose the surface of the material layer 208 to form the passivation layer 210a. The etching back of the conformal passivation layer includes performing a dry etching process. The material layer 208 on the doped layer 206a is then removed, for example, by a wet etching process.

[0029] Continuing to Figure 2G, a thermal process is conducted. Due to the high temperature, dopants in the doped layer 206a diffused to the substrate 200 to form the doped region 212. Concurrently, the doped layer 206a would react with the substrate 200 to form an oxide layer 214. The thermal process is conducted under, for example, an oxygen gas, wherein the flow rate of the oxygen gas is about 10 to 50 liter/min. Further, the thermal process is conducted at about 700 to about 1000 degrees Celsius. The duration of the thermal process is about 10 to 30 minutes. Further, the consumption of the substrate 200 is

about 180 angstroms to about 200 angstroms thick when the substrate 200 reacts with the doped layer 206a to form the oxide layer 214. The aforementioned doped region 212 is subsequently served as the buried plate of the deep trench capacitor.

[0030] Thereafter, as shown in Figure 2H, the oxide layer 214 is removed to form a bottle-shaped deep trench 216. A buried plate of a deep trench capacitor is also formed in the substrate 200 adjacent to the bottle-shaped deep trench 216.

[0031] The subsequent manufacturing process of the present invention further includes forming sequentially a dielectric layer and an electrode layer in the deep trench, wherein the electrode layer, the dielectric layer and the buried plate together complete the formation of a deep trench capacitor. Beside, a conductive layer can be further used to electrically connect the capacitor and the transistor on the substrate to form a memory cell of a dynamic random access memory device.

[0032] In accordance to the fabrication method of the present invention, a polysilicon material layer is used in the place of the conventional photoresist layer to control the dimension of the buried plate. An advantage of using a polysili-

con material is its thickness is easily controlled. Therefore a non-uniformity in the thickness of the photoresist layer leading to inconsistency in the dimension of the buried layer and in the capacitance of the capacitor as commonly occurred in the prior art is prevented.

[0033] Further, the passivation layer formed on the sidewall of the deep trench is thicker by a chemical vapor deposition method than a nitridation method. Therefore, the problem of an insufficient thickness of the passivation formed by a nitridation method, leading to the incapability of resisting the etchant during the etching process is obviated.

[0034] Further, a large quantity of oxygen gas is used in the thermal process to conduct the dopant diffusion and to form the oxide layer concurrently. Therefore, after the oxide layer is removed, a bottle-shaped deep trench can be formed. The present invention can thereby complete the formation of a bottle-shaped deep trench structure and a buried plate of a deep trench capacitor at the same time. As a result, the manufacturing process is simplified and the manufacturing time is reduced.

[0035] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope

or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.